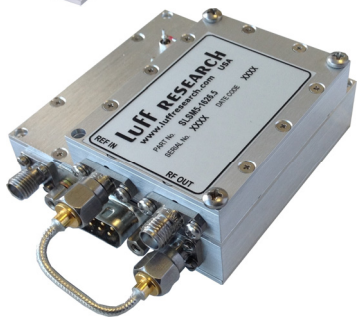
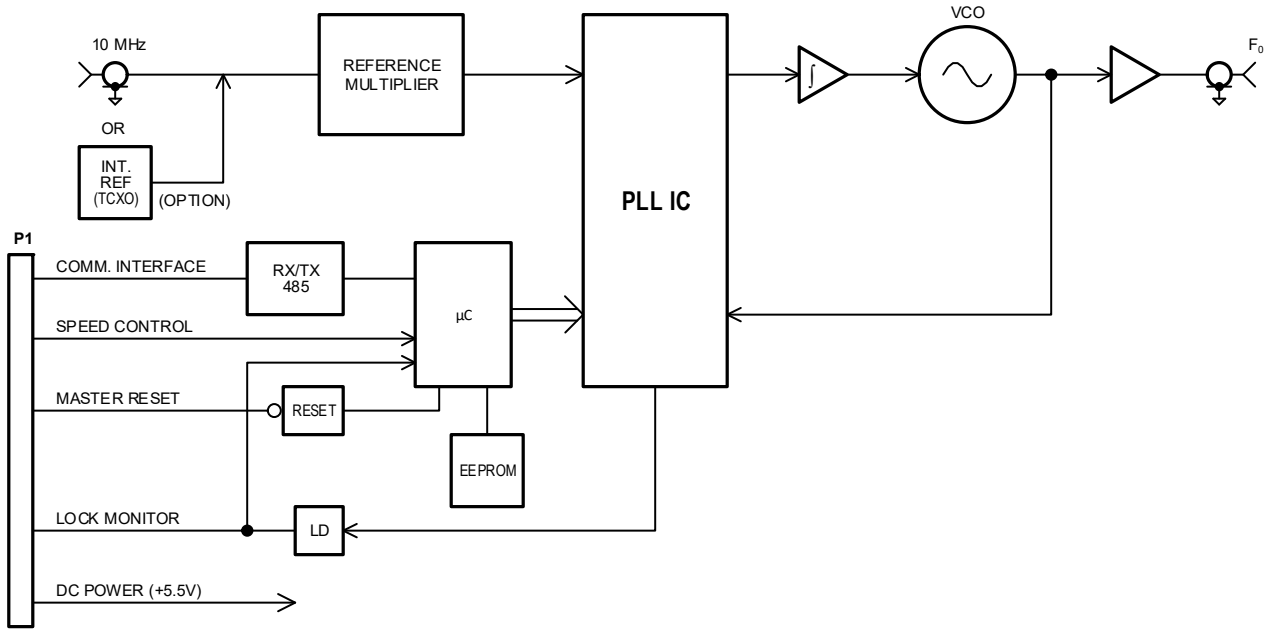
SLSM5 SYNTHESIZER INTERFACE DEFINITION

GENERAL



The SLSM5 synthesizer employs the latest fractional N technology to realize a high performance versatile frequency synthesizer. The SLSM5 architecture makes possible for very wideband synthesizers with 1 kHz step resolution up to 32 GHz. These units offer excellent phase-noise and low spurious performance.

The SLSM5 is ideal for many applications in communications, radar and instrumentation. This synthesizer provides outstanding performance and reliability in a high quality compact unit.



REFERENCE SIGNAL

1. EXTERNAL REFERENCE

The external 10 MHz reference signal should be a good quality signal at a level of 0 dBm ±3dB.

2. INTERNAL REFERENCE

An optional configuration (SLSM5-xxxx-INT) provides an internal 10 MHz TCXO (±0.5ppm -10°C to +70°C). In this configuration the synthesizer will operate on the internal reference only.

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DC POWER AND FREQUENCY CONTROL

The DC power and frequency control is via P1, a 9 pin (MALE) D-SUB connector. The pin-out for this connector is given below. The synthesizer has an internal LDR and filtering however the supplied DC voltage should be from a quality power supply source capable of supplying 650 mA.

CONNECTOR P1	
Pin Number	Description
1	TX+ (out of synthesizer)
2	TX- (out of synthesizer)
3	RX- (into synthesizer)
4	RX+ (into synthesizer)
5	Speed Select Internal pull-up (0=115.2K, 1=9600)
6	+5.5 Vdc ±0.5 V
7	(LD) Lock Detector (note 3)
8	/MR (Master Reset) 0-3V
9	GND

Notes:

1. For 2-wire mode tie together pins 1+4 and 2+3.
2. /MR is the master reset and is active low (0V). Max high (3V)
3. The LD is custom configured for open collector or TTL as indicted on specific product data sheet.

LOCK DETECTOR

The synthesizer status monitoring for phase lock can be done in one of two ways as shown below:

- LD Pin 7 of P1, this lock detector indicates a failed condition and is low when a failure is sensed. The LD is configured as an open collector and is valid for all fault conditions including no reference signal.
- Through polling via the serial interface. However this would not be responsive if the reference is removed.

Please note that monitoring pin 7 does not add noise to the output, while polling via the serial interface can result in spectral degradation.

NON-VOLATILE MEMORY

The SLSM5 has an internal non-volatile memory (EEPROM) device which retains the settings of the last commanded state. The frequency and mute state are saved to this memory. At power up turn on the synthesizer will be restored to the last saved state.

The non-volatile memory (EEPROM) is limited to 1,000,000 write cycles.

HOP MODE FOR CONTINUOUS FREQUENCY ADDRESSING

For applications that require unlimited tuning cycles like continuous band sweeping or random continuous address of the frequency, a hop-frequency command is provided. The hop-frequency command does not save the commanded frequency to the non-volatile memory (EEPROM).

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SERIAL INTERFACE PROTOCOL

Luff Research's Model SLSM5 frequency synthesizers are monitored and controlled through an asynchronous serial interface (UART). The electrical interface is RS485 and can be wired in two or four wire mode. The serial communications operates at either 9600 Baud or 115200 Baud selectable through the interface connector. Additional specifications for the interface are 8 data bits, 1 stop bit, no parity, and no flow control. The protocol is addressable allowing multi-drop communications. The address is selectable through a rotary switch on the unit.

Serial communication occurs **only** with either an external 10 MHz reference or an internal TCXO. The synthesizer serial interface shall operate in a command/response mode. The remote host shall provide the desired frequency setting in ASCII values and the synthesizer shall respond with a command accepted or rejected response. An ASCII 'A' shall be returned if the command is accepted and an ASCII 'R' shall be returned if the command is rejected. The ACK/NACK response shall be followed by a carriage return. The synthesizer output can be turned off or on (mute) through the serial interface. Current status of the synthesizer can also be obtained via the serial interface. Two ASCII characters representing the address setting allow multiple synthesizers to be connected together in RS-422/RS-485 mode. The synthesizer shall only accept & respond to commands that include address values that match the rotary switch (S1) setting (Refer to Figure 1).

Address 0xFF is used as a global address and the unit will always respond to this address. The address in the response will correspond to the actual setting. This feature allows the user to determine the rotary switch setting via the serial interface. This feature cannot be used in multi-drop mode. The unit is shipped with the address set to 01. Care should be taken in setting S1 since it is a plastic screw and can be damaged with an inappropriate metal screw driver.

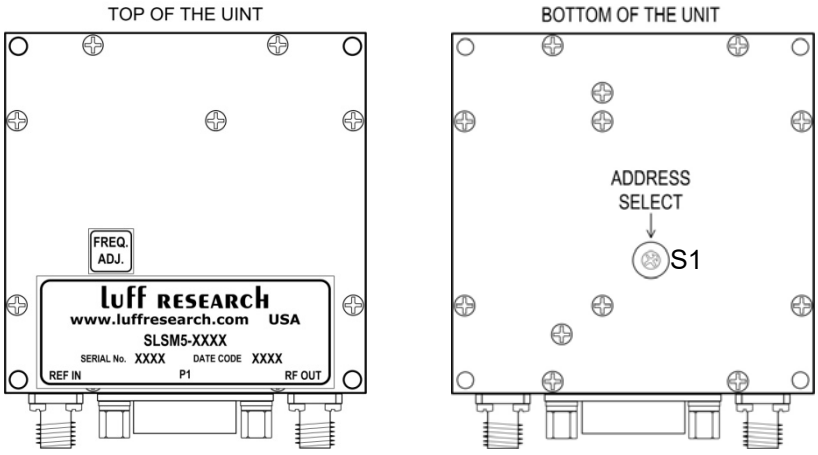

FIGURE 1

There are three independent commands available to control the synthesizer. Please note that at power turn-on, the synthesizer returns to the last state saved in the non-volatile memory.

DEFINITIONS:

All characters are ASCII characters

- >Start of Message HOST to SYNTH
- <Start of message SYNTH to HOST
- ? is the status

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- F is the frequency command; the frequency value is saved to non-volatile memory.
- H is the hop-frequency command; the frequency value is NOT saved to non-volatile memory.
- n1n2 represents address '00' to '0F' as set by S1
- fffffff represents the current frequency in 1 kHz steps.
- L is the lock/unlock condition of the synthesizer, 'L'=Locked; 'U' = Unlocked; 'M' =Muted
- ↵ is the carriage return.
- M is the mute command
- m is a value of '0' or '1'
  '0'=synthesizer output is OFF
  '1'= synthesizer output is ON
- A = accepted
- R = rejected

FREQUENCY COMMAND:

Command: >n_1n_2Fffffff↵
Response: <n_1n_2A
Examples:

Tune to 3.3 GHz and at address 01:
Command: >01F3300000↵
Response: <01A

Error Frequency:
Command: >01F3300↵
Response: <01R

HOP FREQUENCY COMMAND:

Command: >n_1n_2Hffffffff↵
Response: <n_1n_2A
Examples:

Tune to 3.3 GHz and at address 01:
Command: >01H3300000↵
Response: <01A

Error Frequency:
Command: >01H3300↵
Response: <01R

MUTE COMMAND:

Command: >n1n2Mm↵
Response: <n1n2A
Example:

Command: >01M1↵
Response: <01A

STATUS REQUEST:

Command: >n_1n_2?↵
Response: < n_1n_2FffffffL
Example:

Command: >01?↵
Response: <01F3300000L

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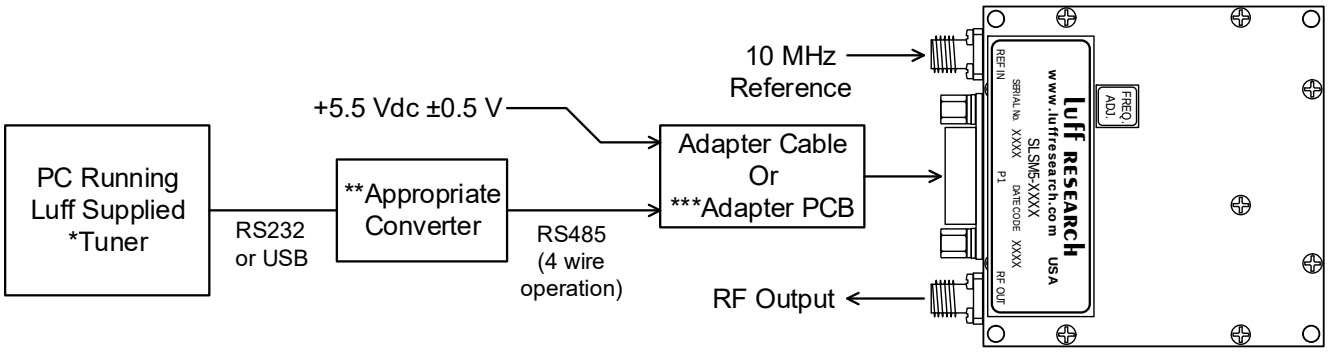
TYPICAL TEST SET-UP



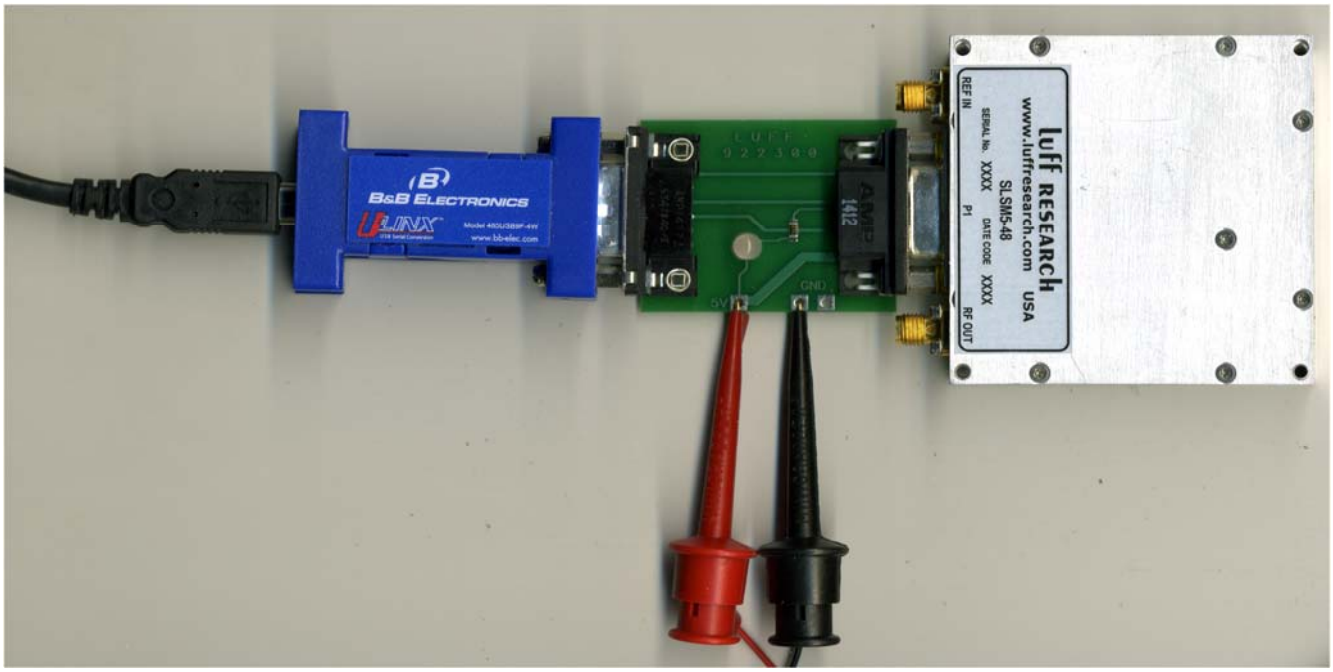
* SLSM5 TUNER (on disc supplied with the unit)

** For RS232 to RS485 - B&B Electronics P/N: 485TBLED or P/N 4WSD9R (along with 485PS) is suggested.

** For USB to RS485 - B&B Electronics P/N: 485USB9F-4W is suggested.

*** Optional PCB adapter (SLSM5-ADP)

Typical SLSM5 Test Setup



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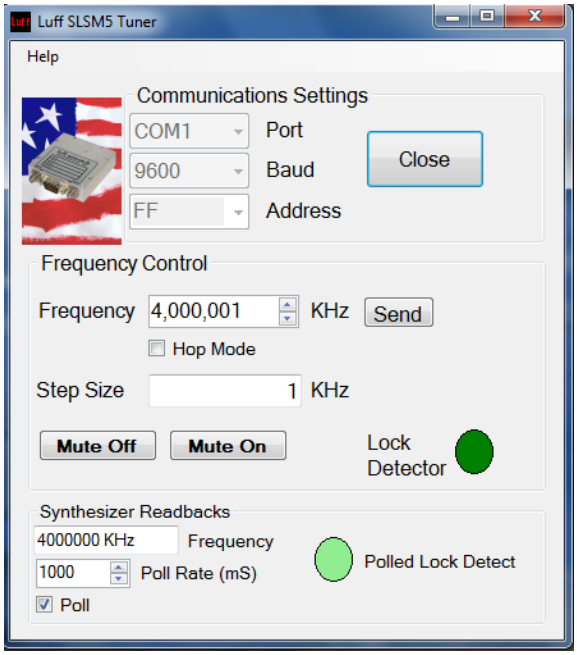
SUPPLIED TUNER SOFTWARE

The synthesizer is supplied with a windows based graphic user interface (GUI) that allows the user to execute frequency control of the synthesizer. The .Net Framework is required for operation of the GUI. Since most PC's and Laptops are provided with a RS232 COM port or USB port the user must provide an appropriate converter for the RS485 transceiver.

SLSM5 Tuner



ADDITIONAL NOTES

The SLSM5 is the most current synthesizer implementation of the fractional-N architecture. The resulting design offers many advantages in performance, size and cost. The following two points are noted:

(1) The output frequency accuracy varies slightly, for example at 4 GHz the output frequency accuracy is actually +2.9··· Hz.

(2) This design utilizes techniques which result in <-60 dBc spurious through most of the band. There may be a small set of frequencies (out of millions) where due to an anomaly in the fractional N process the spurs are >-60 dBc. At these locations for the most part the <-60 dBc level can be realized by shifting the frequency by 1 or 2 kHz.

For technical support please contact Luff Research directly at:
Phone: 516-358-2880 or E-mail to: sales@luffresearch.com

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